

AMENDMENT

Serial Number: 10/585,680

Filing Date: July 10, 2006

Title: METHOD AND APPARATUS FOR PARTITIONING PROGRAMS TO BALANCE MEMORY LATENCY

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Dkt: P22886/INT.P036

**IN THE SPECIFICATION**

Please replace paragraph [0032] with the following paragraph.

[0032]           The code partitioning unit 300 includes an evaluation unit 350. The evaluation unit 350 determines whether ~~the~~a ~~computed~~weight for executing the instructions assigned to the upstage stream or the downstream stage exceeds a predetermined value. If the ~~computed~~weight required for executing the instructions in the upstream stage or the downstream stage exceeds a predetermined value, a new number of desired upstream nodes or a new number of desired downstream nodes is determined. According to an embodiment of the code partitioning unit 300, the new number may include one less number of desired upstream nodes or number of desired downstream nodes.

Please replace paragraph [0038] with the following paragraph.

[0038]           At 405, the remaining instructions are assigned. According to an embodiment of the present invention, the remaining instructions may be assigned while trying to balance a ~~computed~~weight among the pipelined stages, or using other techniques.

Please replace paragraph [0051] with the following paragraph.

[0051]           At 604, it is determined whether ~~the~~a ~~computed~~weight for executing the instructions assigned to the upstage stream exceeds a predetermined value. If the ~~computed~~weight required for executing the instructions in the upstream stage exceeds a predetermined value, control proceeds to 605. If the ~~computed~~weight required for executing the instructions in the upstream stage does not exceed the predetermined value, control proceeds to 606.

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Please replace paragraph [0057] with the following paragraph.

[0057] At 704, it is determined whether ~~the~~a computed weight for executing the instructions assigned to the downstage stream exceeds a predetermined value. If the computed weight required for executing the instructions in the downstream stage exceeds a predetermined value, control proceeds to 705. If the computed weight required for executing the instructions in the downstream stage does not exceed the predetermined value, control proceeds to 706.

Please replace paragraph [0070] with the following paragraph.

[0070] Assuming that the computed weight of instructions (1), (2), (5), and (6) does not exceed a predetermined value, the assignments made at 602 and 603 are utilized.

Please replace paragraph [0081] with the following paragraph.

[0081] Assuming that the computed weight of instructions (1), (2), (3), (5), and (6) does not exceed a predetermined value, the new assignments made at 602 is utilized.

Please replace paragraph [0089] with the following paragraph.

[0089] Referring back to Figure 4, at 405, the remaining instructions are assigned. According to an embodiment of the present invention, the remaining instructions may be assigned while trying to balance a computed weight among the pipelined stages, or using other techniques. In this example, instructions (4) and (8) are assigned to the upstream stage, and instructions (7),

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(9), and (11) are assigned to the downstream stage to generate the exemplary pipelined program with balanced memory latency as shown in Figure 11.

Please delete paragraphs [0074]-[0077].

Please replace paragraph [0078] with the following paragraph.

[0078] Referring back to Figure 6, the ~~third~~second memory access chain 3->10->12 is now partitioned to the upstream stage. At 601, the  $\text{DesiredLengthofUpstream} = N/d = 3/2 = 1.5$ , which rounds to 2.

Please replace paragraph [0084] with the following paragraph.

[0084] Referring back to Figure 6, the ~~fourth~~third memory access chain 3->12 is now partitioned to the upstream stage. At 601, the  $\text{DesiredLengthofUpstream} = N/d = 2/2 = 1$ .